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MILES & STOCKBRIDGE P.C.
1751 PINNACLE DRIVE
SUITE 500
McLean, VA 22102-3833

EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	11

DATE MAILED: 05/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/242,974	UGON, MICHEL	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 20-50 have been considered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 20, 21, 23, 24, 27-36, 40, 41, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin, U.S. Patent Number 5,361,337 (herein referred to as Okin) in view of Fletcher et al., U.S. Patent Number 5,012,409 (herein referred to as Fletcher).

5. Referring to claim 20, Okin has taught an unpredictable microprocessor or microcomputer comprising:

a. A processor (Okin column 1, line 17).

b. A first working memory (Okin column 4, lines 12-26 and Figure 4).

c. A main memory containing a main program (Okin column 2, lines 8-20) and a secondary program (Okin column 2, lines 8-20).

d. A second working memory (Okin column 4, lines 12-26 and Figure 4)

e. Switching means for switching, while the programs are running, from one of the two working memories to the other working memory, while saving the contents of the two working memories (Okin column 3, lines 36-44).

f. Access registers associated with each memory (Okin column 4, lines 7-12 and Figure 4).

g. Said switching means comprising at least one first block of registers for storing the operating context of the programs in the main memory (Okin column 4, lines 12-26 and Figure 4)

h. A switching circuit for enabling one of the working memories and the access registers associated with each memory and controlled by said switching circuit (Okin column 4, lines 4-26 and Figure 4).

6. Okin has not taught the main memory contains an operating system. Fletcher has taught the main memory contains an operating system (Fletcher column 1, lines 16-18). It would have been obvious to a person of ordinary skill in the art to incorporate the operating system in main memory, because the processor requires it to coordinate processes. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the operating system in main memory, of Fletcher, in the device of Okin to coordinate processes.

7. Referring to claim 21, Okin has taught the microprocessor or microcomputer further including a second block of registers for storing the operating context of the secondary program (Okin column 4, lines 12-26 and Figure 4).

8. Referring to claim 23, Okin has not taught the main program can enable or inhibit the switching mechanism or mechanisms by loading the switching circuit for switching and enabling the working memories and blocks of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program. Fletcher has taught the main program can enable or inhibit the switching mechanism or mechanisms by loading the switching circuit for switching and enabling the working memories and blocks of storage registers associated with each respective working memory, and storing, respectively, the operating context of the programs in the main memory and the operating context of the secondary program (Fletcher column 1, lines 16-20 and 33-44). In regards to Fletcher, the program, or task, is written from instructions made available and understood by the operating system. It would have been obvious to a person of ordinary skill in the art to incorporate the main program of Fletcher, because a main program is needed to control the processor's function. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the main program of Fletcher for control over the processor.

9. Referring to claim 24, Okin has not taught the second working memory and its access registers are substituted for the working memory and its access registers in utilization by a main program. Fletcher has taught the second working memory and its access registers are substituted for the working memory and its access registers in utilization by a main program (Fletcher column 1, lines 16-20 and 36-44). It would have been obvious to a person of ordinary skill in the art to incorporate the above, because the main program controls the generating and switching of processes and its resources. Therefore it would have been obvious to a person of ordinary skill

in the art at the time this invention was made to incorporate the above, as taught by Fletcher, in the device of Okin.

10. Referring to claim 27, Okin has not taught the means for switching working memories is controlled by the processor and its program, by the random interrupt system, by a timer, or by any combination of at least two of the three named elements. Fletcher has taught the means for switching working memories is controlled by the processor and its program, by the random interrupt system, by a timer, or by any combination of at least two of the three named elements (Fletcher column 1, lines 12-20). It would have been obvious to a person of ordinary skill in the art incorporate the switching means of Fletcher, because there must be a way to control when the tasks are switching from one to another without losing the context of the current task. Therefore, It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the switching means of Fletcher in the device of Okin to control the switching of tasks.

11. Referring to claim 28, Okin has not taught the means for switching working memories is enabled by being loaded by the processor running a main program sequence. Fletcher has taught the means for switching working memories is enabled by being loaded by the processor running a main program sequence (Fletcher column 1, lines 16-20 and 36-44). It would have been obvious to a person of ordinary skill in the art to incorporate the means for switching of Fletcher, because the main program controls the processor's function, which includes the switching means. Therefore, It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the means for switching as taught by Fletcher in the device of Okin.

12. Referring to claim 29, Okin has taught the secondary program uses a working space identical to that of the main program in the main memory (Okin column 2, lines 8-20). It is implied that the working space is identical, since they use the same cache.

13. Referring to claim 30, Okin has taught the secondary program uses a working space smaller than that of the main program (Okin column 2, lines 8-20). It is inherent that the working space is smaller, since it uses the same cache as the main program.

14. Referring to claim 31, Okin has taught the switching means carry out the substitution of the memories and the associated contexts within the execution cycle of the instruction from the microprocessor (Okin column 4, lines 13-20).

15. Referring to claim 32, Okin has taught the secondary program does not modify general operating context of the main program in order to allow the main program to return without having the reestablish said context (Okin column 4, lines 4-26 and 44-48).

16. Referring to claim 33, Okin has taught the context of the main program is reestablished either automatically by the secondary program or automatically by the switching means before returning control to the main program (Okin column 4, lines 4-26 and Figure 4).

17. Referring to claim 34, Okin has taught means for substituting the memory of the secondary program for the memory of the main program (Okin column 4, lines 4-26). It is inherent since the main program can choose where to read and write.

18. Referring to claim 35, Okin has taught the main program can use the first working memory and/or the second working memory alternately or simultaneously (Okin column 4, lines 4-26). It is inherent since the main program can choose where to read and write.

19. Referring to claim 36, Okin has taught loading of the switching circuit makes it possible to mask or unmask de-correlating interrupts (Okin column 4, lines 4-26). It is inherent to be able to mask or unmask interrupts, because the switching means needs to be able to identify and use interrupts when they occur, randomly or not.

20. Referring to claim 40, Okin has not taught the main program is adapted to enable or inhibit the switching mechanism or mechanisms by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory. Fletcher has taught the main program is adapted to enable or inhibit the switching mechanism or mechanisms by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory (Fletcher column 1, lines 16-20 and 36-44). It would have been obvious to a person of ordinary skill in the art to incorporate the main program of Fletcher, because the main program controls the processor's function, which includes the switching mechanism. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the main program as taught by Fletcher in the device of Okin.

21. Referring to claim 41, Okin has taught the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory and the associated access registers of the first memory (Okin column 4, lines 4-26 and Figure 4).

22. Referring to claim 50, Okin has taught the means for switching the working memories is confirmed by loading from the processor executing a main program sequence (Okin column 4, lines 4-26 and Figure 4).

23. Claims 22, 25, 26, 37, 39, and 42-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin in view of Fletcher as applied to claims 20, 21, and 23 above, and further in view of Griffin, III et al., U.S. Patent Number 5,249,294 (herein referred to as Griffin).

24. Referring to claim 22, Okin has not taught the microprocessor further including means for de-correlating the running of the programs from an isochronous clock. Griffin has taught means for de-correlating the running of the programs from an isochronous clock (Griffin columns 1-2, lines 36-2). It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because it would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

25. Referring to claim 25, Okin has not taught the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, a random interrupt for descynchronizing the running of the programs in the processor, by randomly jumping to the secondary program. Griffin has taught the de-correlating means comprise a random number generator for triggering, via an interrupt circuit, a random interrupt for descynchronizing the running of the programs in the processor, by randomly jumping to the secondary program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the random number generator is inherent in order to determine the random duration interval and the interrupt circuit and interrupt are inherent in order to jump to the interim routines in the middle of a process. It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because it would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at

the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

26. Referring to claim 26, Okin has not taught the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program. Griffin has taught the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermined process. It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because there must be a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

27. Referring to claim 37, Okin has taught that an interrupt triggered by the secondary program effects return to the main program after the switching register has been properly loaded, by executing an instruction of the main program or the secondary program, in order to unmask the interrupts (Okin column 4, lines 4-36). It is inherent that, while the interrupt is being processed, the pipeline will continue until the interrupt is decoded.

28. Referring to claim 39, Okin has not taught the microprocessor further including means of de-correlating the run-through of the programs with respect to an isochronal clock. Griffin has taught means of de-correlating the run-through of the programs with respect to an isochronal

clock (Griffin columns 1-2, lines 36-2). It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because it would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

29. Referring to claim 42, Okin has not taught the de-correlating means comprise a random generator. Griffin has taught the de-correlating means comprise a random generator (Griffin columns 1-2, lines 58-2). It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because it would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to improve security.

30. Referring to claim 43, Okin has not taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, the triggering an interruption to return from the secondary program to the main program. Griffin has taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, the triggering an interruption to return from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermine process. It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because there must be a way to return to the main program to complete the processor's task.

Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

31. Referring to claim 44, Okin has taught the means of switching the working memories is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or a combination of at least two out of the three named elements (Okin column 3, lines 28-44).

32. Referring to claim 45, Okin has not taught the main program is adapted to enable or inhibit the switching mechanism or mechanisms by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory. Fletcher has taught the main program is adapted to enable or inhibit the switching mechanism or mechanisms by loading the switching circuit of working memories and of the memorization register blocks associated with each respective working memory (Fletcher column 1, lines 16-20 and 36-44). It would have been obvious to a person of ordinary skill in the art to incorporate the main program of Fletcher, because the main program controls the processor's function, which includes the switching mechanism. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the main program as taught by Fletcher in the device of Okin.

33. Referring to claim 46, Okin has taught the second working memory and the associated access registers of the second working memory are adapted to be replaced in the use thereof by a main program, with said first memory and the associated access registers of the first memory (Okin column 4, lines 4-26 and Figure 4).

34. Referring to claim 47, Okin has taught the means of switching the working memories is controlled, either by one of the microprocessors and the program thereof, the random interruption system, a time counter, or by a combination of at least two out of the three named elements (Okin column 3, lines 28-44).

35. Referring to claim 48, Okin has not taught the interruption circuit triggers the random generator to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program. Griffin has taught the interruption circuit triggers the random generator to thereby trigger the random interrupt to desynchronize execution of the programs in the processor, by random connection to the secondary program (Griffin columns 1-2, lines 36-2). It would have been obvious to incorporate the interruption circuit as taught by Griffin, because it would prevent "clocks attacks" from compromising the system (Griffin Abstract, lines 1-8). Therefore, it would have been obvious at the time this invention was made to incorporate interruption circuit as taught by Griffin in the device of Okin to improve security.

36. Referring to claim 49, Okin has taught the means of switching the working memories is controlled by one of the microprocessors and the program thereof, the random interruption system, a time counter or by a combination of at least two of the three named elements (Okin column 3, lines 28-44). It is inherent that an interrupt can only occur when an interrupt is introduced by a source. Okin has not taught the de-correlating means comprise a time counting system independent from the processor for enabling, at the end of a time count, the triggering an interruption to return from the secondary program to the main program. Griffin has taught the de-correlating means comprise a time counting system independent from the processor for

enabling, at the end of a time count, the triggering an interruption to return from the secondary program to the main program (Griffin columns 1-2, lines 58-11). In regards to Griffin, the counting system is inherent to determine the end of the random duration of the interim routine and triggering the interrupt is inherent to return to the predetermine process. It would have been obvious to incorporate the means for de-correlating as taught by Griffin, because there must be a way to return to the main program to complete the processor's task. Therefore, it would have been obvious at the time this invention was made to incorporate means for de-correlating as taught by Griffin in the device of Okin to be able to return to the main program.

37. Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okin in view of Fletcher as applied to claim 20 above, and further in view of Takagi, U.S. Patent Number 5,280,618 (herein referred to as Takagi). Okin has not taught the microcomputer or microprocessor is embodied in a monolithic integrated circuit. Takagi has taught the microcomputer or microprocessor is embodied in a monolithic integrated circuit (Takagi column 1, 14-22). It would have been obvious to a person of ordinary skill in the art to incorporate the monolithic integrated circuit of Takagi, because it broadens the number of applications the computer or processor may be used for. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the monolithic integrated circuit of Takagi in the device of Okin to increase usefulness.

Response to Remarks

38. Applicant's arguments filed 20 March 2003, paper number 10 have been fully considered but they are not persuasive.

39. The examiner's objection to the Oath/Declaration has been withdrawn.

40. The examiner's objection to the claims has been withdrawn in favor of the amended claims.

41. The examiner's rejection under 35 U.S.C § 112 has been withdrawn in favor of the amended claims.

42. Applicant argues on page 11 that the title "is aptly descriptive of the invention." This has not been found persuasive. The examiner's objection to the title stands. The title of the invention, "Unpredictable Microprocessor or Microcomputer", is not descriptive of the invention. A person of ordinary skill in the art would not know clearly what the claimed invention is. Please see MPEP §606 and §606.01.

43. Applicant argues on page 13, paragraph 1 essentially that:

> "switching, at random interrupts, between two working memories. Okin discloses a processor switching between processes, and not a processor switching between memories as is taught by the Applicant."

44. This has not been found persuasive. It is well known in the art that when switching processes, memories must be switched as well. Okin has disclosed, as well, that when switching processes, state elements are switched (Okin column 2, lines 23-36 and Figure 4). The state elements include memory elements, such as registers (Okin column 3, lines 13-18). Also, when processes switch, the memory where the process instructions are being provided from are switched and these are working memories as well.

45. Applicant argues on page 13, paragraph 2 essentially that, "The object of the Okin apparatus is to improve processor efficiency, while the object of the present invention is to improve processor security." This has not been found persuasive. In response to applicant's

argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., object of the present invention is to improve processor security) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

46. Applicant argues on pages 13-14, paragraphs 3-1 essentially that, "Fletcher does not teach technical features for cooperation between an unpredictable processor and an operating system..." and "Fletcher does not disclose any feature to improve security in a processor." This has not been found persuasive. Fletcher was relied upon to teach that an operating system is necessary to define and coordinate processing activities within a processor and system (Fletcher column 1, lines 16-18). Also, in response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., specific technical features for cooperation between an unpredictable processor and an operating system and to improve security in a processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

47. Applicant argues on page 14, paragraph 2 essentially that "...main program controls the switching mechanism, and not necessarily a processor." This has not been found persuasive. Fletcher has taught the operating system and main program are necessary to define and coordinate processing activities within a processor and system (Fletcher column 1, lines 16-18 and 33-44). The switching mechanism is part of the system, which in Okin's case is the

processor (Okin Figure 4). Therefore, the switching mechanism is controlled by the main program.

48. Applicant argues on page 15, paragraph 1 essentially that:

> "Applicant believes the Examiner relies on improper 'pick and choose' for attempting to reach the claimed invention, but there is no suggestion to combine these references or that the references can be so combined to produce the result of the claimed combinations."

49. This has not been found persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the suggestion to combine found on page 9, paragraph 29, lines 3-4 in the original Office Action was to prevent "clock attacks" from compromising the system, thereby making the system more secure, as disclosed in Griffin on column 1, lines 11-14 and 37-45.

50. Applicant argues on page 15, paragraphs 2-3 essentially that:

> "...Okin does not teach that the de-correlating means comprise a time counting system independent from the processor for, after the time count, triggering an interrupt for returning from the secondary program to the main program...

...Okin does not disclose means of de-correlating the run-through of the programs with respect to an isochronal clock."

51. This has not been found persuasive. Okin was not relied upon to teach the details above of claims 26 and 39, as can been seen in the Office Action on page 10, paragraphs 31 and 33. Griffin was relied upon. Also, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

52. Applicant argues on page 16, paragraph 3 essentially that "Takagi does not disclose any feature to improve security in a processor. Again, there is no suggestion to combine the references." This has not been found persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., feature to improve security in a processor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Also, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the suggestion to combine references, found on

page 14, paragraph 14, lines 7-8 of the original Office Action, was to broaden the number of applications the computer or processor is used for, as disclosed in Takagi on column 1, lines 14-22.

Conclusion

53. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

54. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

56. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

57. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

May 22, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100